Amendments to the claims:

1 (Original) A packet buffer write system comprising:

a descriptor status array having n locations, a first end and a second end, each of said n locations having the value free or used;

a packet buffer comprising a descriptor memory having said n storage locations and a data segment memory having said n storage locations;

a plurality said n of unique packet memory slots, each said packet memory slot having a unique one of said descriptor status array locations, a unique one of said descriptor memory locations, and a unique one of said data segment memory locations, said packet memory slots thereby uniquely addressable by each said descriptor status array location;

a next host controller which returns a slot-a pointer to said free value in said descriptor status array by searching from said first end of said descriptor status array;

a next MAC controller which returns a slot-b pointer to said free value in said descriptor status array by searching from said second end of said descriptor status array;

a host Tx controller coupled to said next host controller, said host Tx controller receiving host Tx Data including a Tx header and Tx payload and placing said Tx header into said descriptor storage slot-a, and placing said Tx payload into said data segment slot-a, said host Tx controller thereafter causing said next host controller to change said slot-a descriptor status array location value from said free to said used;

a MAC Rx controller coupled to said next MAC controller, said MAC Rx controller receiving MAC Rx Data including an Rx header and Rx payload and placing said Rx header into said descriptor storage slot-b, and placing said Rx payload into said data segment slot-b, said MAC Rx controller thereafter causing said next MAC controller to change said slot-a descriptor status array location value from said free to said used.

2(Original) The packet buffer write system of claim 1 where said descriptor status array is a linear array of said n bits of data, each said bit having said value free or said value used.

3(Original) The packet buffer write system of claim 1 where said packet buffer memory comprising said data segment location is size s and said descriptor location is size d.

4(Original) The packet buffer write system of claim 3 where one of said n memory slots is slot k, and said packet buffer memory is in read-write memory, and said descriptor memory address is said k multiplied by said d.

5(Original) The packet buffer write system of claim 3 where one of said n memory slots is slot k, and said data segment memory is in read-write memory, and said data segment memory address is said k multiplied by said s.

6(Original) The packet buffer write system of claim 1 where said descriptor status array is separate from said packet buffer.

7(Original) The packet buffer write system of claim 1 where said descriptor status array is in a logic device and said packet buffer is in a memory device.

8(Original) The packet buffer write system of claim 1 where each said descriptor status array location is one bit, each said descriptor memory location is 256 bytes, and each said data segment memory is 256 bytes.

9(Original) The packet buffer write system of claim 1 where each said descriptor memory location includes a pointer to next.

10(Original) The packet buffer write system of claim 1 where said descriptor memory location includes provision for storing a packet source address.

11(Original) The packet buffer write system of claim 1 where said descriptor memory location includes provision for storing a packet destination address.

12(Original) The packet buffer write system of claim 1 where said descriptor memory location includes provision for storing a pointer to a next descriptor.

13(Original) The packet buffer write system of claim 1 where said descriptor memory location includes a provision for storing a packet type field.

14(Original) The packet buffer write system of claim 1 where said descriptor memory location includes provision for storing a packet length field.

15(Original) The packet buffer write system of claim 1 where said data segment memory includes provision for storing packet data.

16(Original) The packet buffer write system of claim 1 where said packet memory slots is organized into separate queues, each said queue comprising a plurality of said packet memory slots, each said queue for handling a priority.

17(Original) The packet buffer write system of claim 16 where said priority is based on a type field in said packet header.

18(Original) The packet buffer write system of claim 16 where said priority is based on information in the header of a received packet.

19(Original) The packet buffer write system of claim 16 where one said priority queue receives handling by said packet buffer write system before another said priority queue.

Claims 20-54 are cancelled.